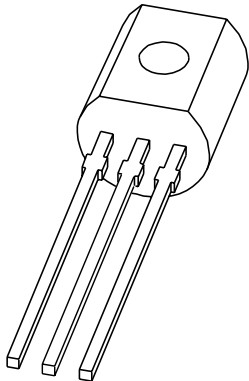


DATA SHEET



PBSS5350S

50 V low V_{CEsat} PNP transistor

Product specification
Supersedes data of 2001 Nov 19

2004 Aug 20

50 V low V_{CEsat} PNP transistor

PBSS5350S

FEATURES

- High power dissipation (830 mW)
- Ultra low collector-emitter saturation voltage
- 3 A continuous current
- High current switching
- Improved device reliability due to reduced heat generation.

APPLICATIONS

- Medium power switching and muting
- Linear regulators
- DC/DC convertor
- Supply line switching circuits
- Battery management applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers).

DESCRIPTION

PNP low V_{CEsat} transistor in a SOT54 plastic package.
NPN complement: PBSS4350S.

MARKING

TYPE NUMBER	MARKING CODE
PBSS5350S	S5350S

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	-50	V
I_C	collector current (DC)	-3	A
I_{CM}	peak collector current	-5	A
R_{CEsat}	equivalent on-resistance	<150	m Ω

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

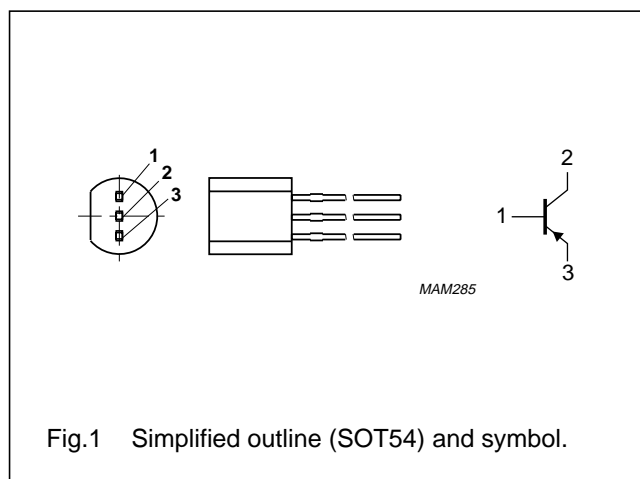


Fig.1 Simplified outline (SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	-	-60	V
V_{CEO}	collector-emitter voltage	open base	-	-50	V
V_{EBO}	emitter-base voltage	open collector	-	-6	V
I_C	collector current (DC)		-	-3	A
I_{CM}	peak collector current		-	-5	A
I_{BM}	peak base current		-	-1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1	-	830	mW
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		-65	+150	$^\circ\text{C}$

Note

1. Device mounted on a printed-circuit board, single sided copper, tinplated and standard footprint.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	150	K/W

Note

1. Device mounted on a printed-circuit board, single sided copper, tinplated and standard footprint.

CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

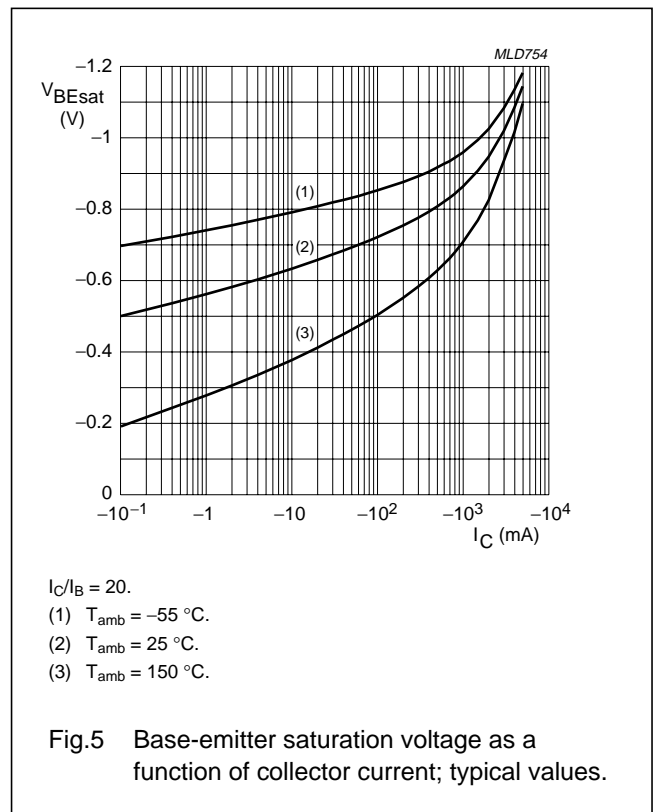
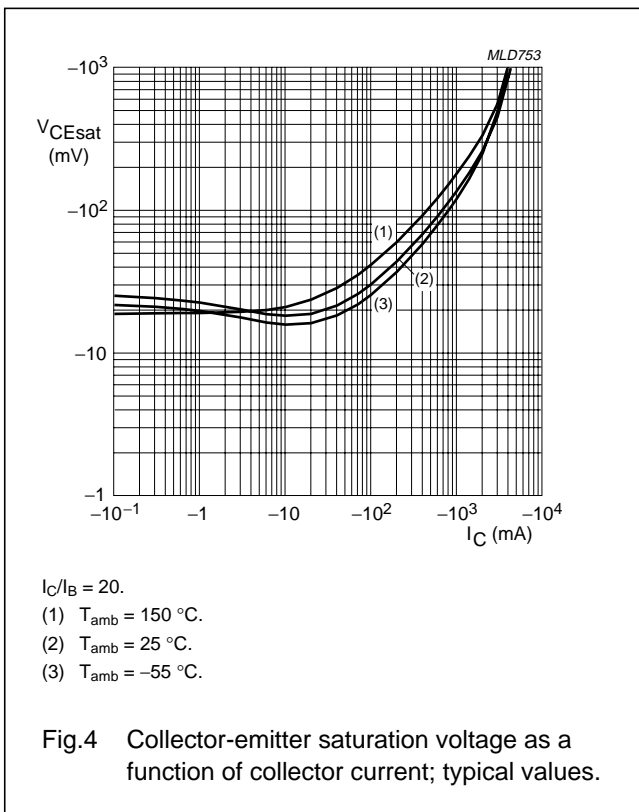
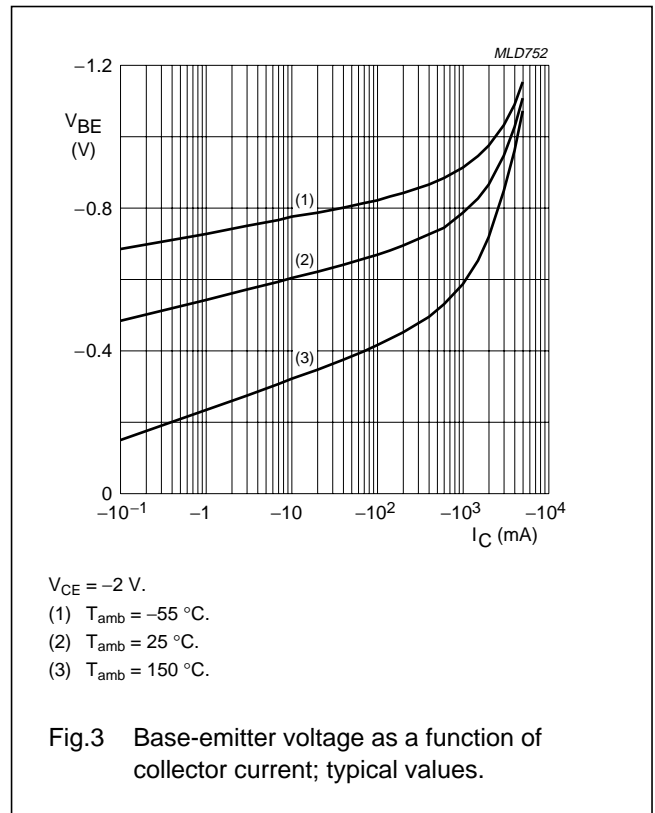
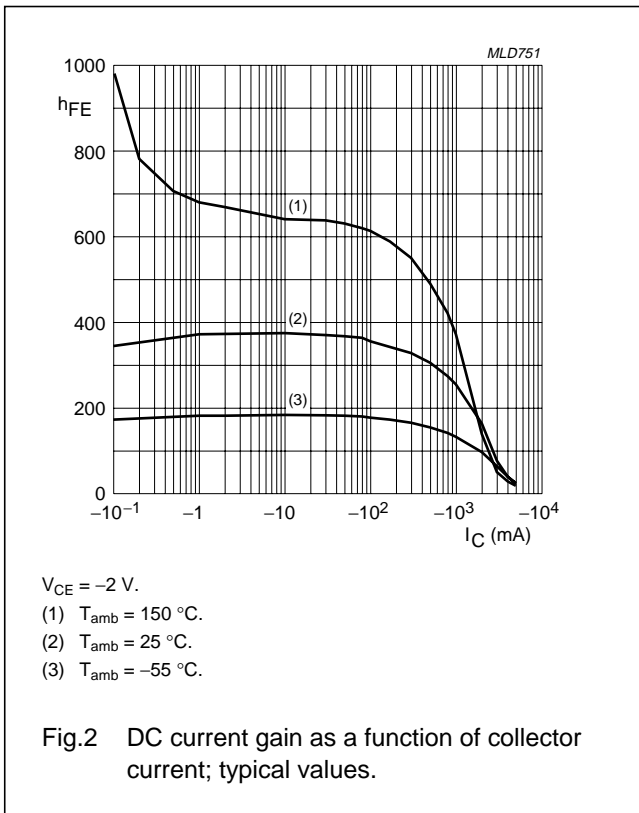
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -50\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	200	–	–	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}; \text{note 1}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–	–100	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	–180	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–300	mV
R_{CEsat}	equivalent on-resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	120	<150	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–1.2	V
V_{BE}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	–	–	–1.1	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	100	–	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	40	pF

Note

1. Pulse test: $t_p \leq 300\ \mu\text{s}$; $\delta \leq 0.02$.

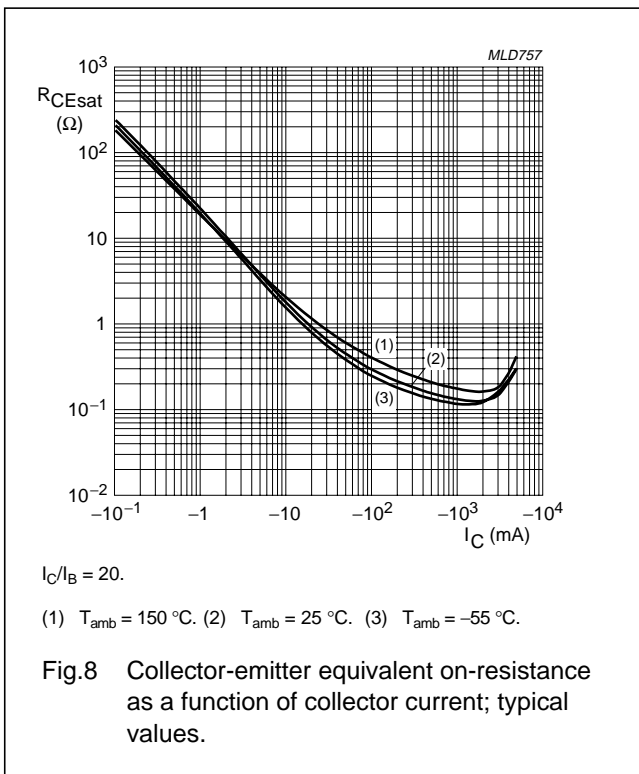
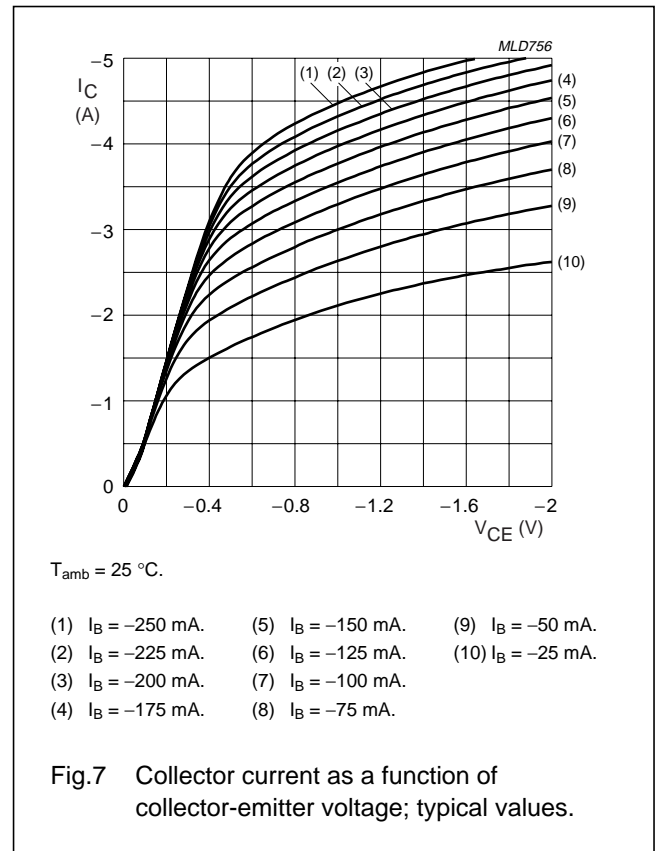
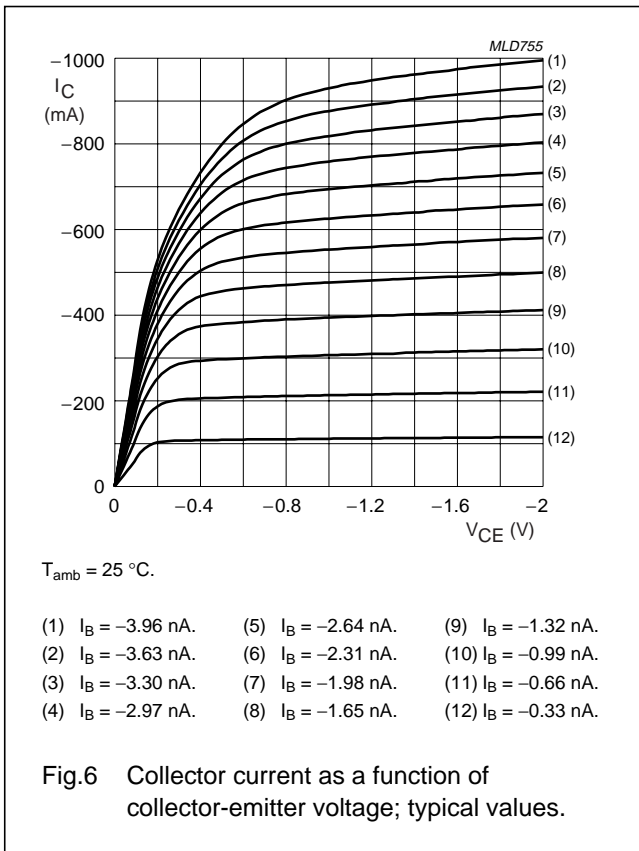
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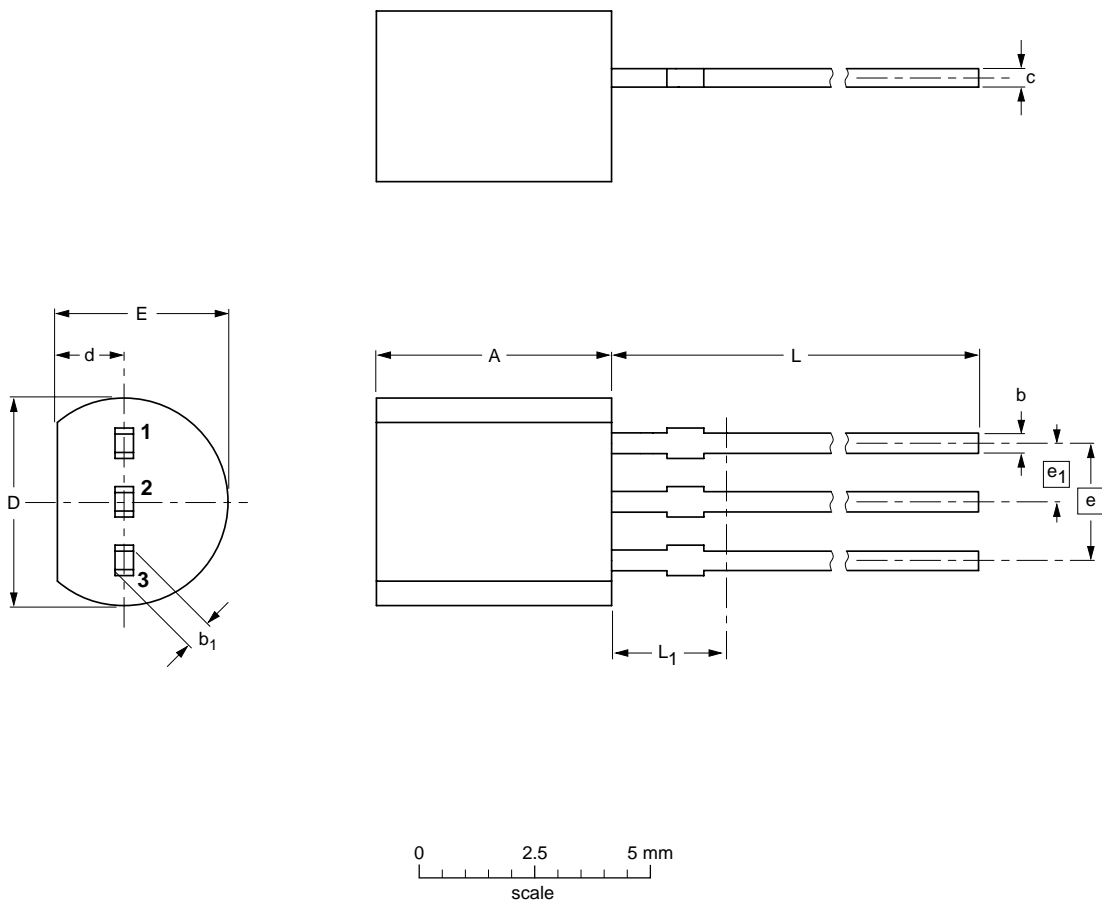
50 V low V_{CEsat} PNP transistor

PBSS5350S

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

50 V low V_{CEsat} PNP transistor

PBSS5350S

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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